NanoXplore

IC LAYOUT DESIGN ENGINEER F/M

NanoXplore is a pioneer in design and development of space-grade FPGA and e-FPGA located in Paris and Montpellier. As a rapidly growing company, NanoXplore is looking to continue building its software and hardware teams.

We are currently hiring an IC layout design engineer who will join our hardware R&D team located in Paris. This person will contribute to the development of NanoXplore's standard cell and IP libraries at 28nm and below.

MISSION

- Analysis and synthesis of specifications.
- Schematic design of library cells and characterization.
- Layout of library cells following integration specifications.
- DRC/LVS check of the library.

REQUIRED SKILLS

- Experience in transistor-level design (FINFET and/or FDSOI).
- Experience with Cadence Virtuoso suite, SPICE simulator and Mentor Calibre DRC/LVS.
- Strong understanding of physical constrains in IC design layout for area optimization and yield improvement.

PROFIL

- Engineering degree or relevant experience.
- Good communication (oral and writing) skills in French.
- Availability ASAP**.**

COMPANY

Join our highly motivated team and be part of our success story "à la francaise," in a company with a start-up mentality. We have always believed that our limits are drawn by your motivation. Always attentive to the wellbeing of its employees, NanoXplore allows you to grow and to develop your skills in a quick-paced, reactive working environment. Have any questions about what do we do? The Company? Daily life? Please contact us at careers@nanoxplore.com.

SUMMARY

- Contract: CDI – full-time
- Location: SEVRES - Île-de-France
- Experience: minimum 5 years
- Salary: based on your profile.